REMARKS

This responds to the Office Action dated on December 21, 2006.

Claims 1-3, 7, 10, 13, 17-22, 24, 35-39 and 41 are amended, claims 4, 23, 26-34 and 40 are canceled, and claims 43-45 are added; as a result, claims 1-3, 5-22, 24, 25, 35-39 and 41-45 are now pending in this application.

Claim Objections

Claims 1-6, 22-25, 28-31, 32-34 and 39-42 were objected to due to informalities. Specifically, for example, the Examiner stated that acronyms (such as 'ISDS' in claim 1, or 'ISDC' in claim 3) should not be used to abbreviate key terms or phrases until they are explicitly defined previously within the claim or a claim to which it depend (Office Action, p. 3, lines 1-3). The Examiner also stated that, with respect to claim 23, the term "system cache identifier" is not defined or disclosed in the specification.

Claims 1, 3, 13, 22 and 39 have been amended to more correctly define Applicant's claimed invention as required by the Examiner.

With respect to the limitation of 'system cache identifier' in claim 23, claim 23 has been canceled. Newly added limitation of 'cell identifier' in amended claim 22 is fully supported from Applicant's Specification. For example, as noted at p. 13, line 21 and p. 14, line 23 through p. 15, line 1, Applicant teaches that a cell (306) within a selected coherence buffer (302A – 302B) is selected by the cell number indicated in the SELECT_CELL field (502). Reconsideration is respectfully requested.

Drawings

The drawings were objected to as failing to comply with 37 C.F.R. 1.84(p)(4) because reference character "112" in Figure 1 has been used to designate both the Memory Unit and the I/O interface.

Figure 1 has been amended so that a reference character "118" is used to designate the Memory Unit.

§101 Rejection of the Claims

Claims 35-42 were rejected under 35 U.S.C. § 101 because claims are not limited to tangible embodiments. Specifically, the Examiner stated that the claimed medium is directed to intangible embodiments because the relevant portion of the Specification (p. 8, line 21 through p. 9, line 3) is defined to include such intangible embodiments as electrical, optical propagated signals and carrier waves, etc. (Office Action, p. 3, #5).

The Specification has been amended to clarify the description as required by the Examiner. Reconsideration is respectfully requested.

§103 Rejection of the Claims

Claims 1-2, 10-12, 18-21 and 35-38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Michael et al. (U.S. Publication No. 2002/0002659A1) and further in view of Joseph et al. (U.S. Patent No. 6,405,292) and Carpenter et al. (U.S. Patent No. 6,266,743).

Applicant's invention claimed in claim 1, 10, 18 and 35 is about a method and apparatus for maintaining cache coherence among a plurality of system caches throughout one or more nodes. Specifically, as noted at p. 2, lines 5-8 of the Specification, Applicant's claimed invention pertains to, for example, reducing memory overhead in a traditional full map bit-vector directory.

To accomplish this purpose, Applicant claims using an Ingrained Sharing Directory Storage (ISDS). The ISDS allows Applicant to map a bit-vector with two or more entries into as many cells. To do this, Applicant teaches that the ISDS has a plurality of cells and that each cell has several entries where each entry corresponds to one memory line. Applicant also claims that **each of the cells maintains a dynamic full map of shared lines cached in a given set of one of the plurality of system caches** throughout the one or more nodes. In other words, each of the plurality of cells is associated with one of the plurality of system caches Therefore, under Applicant's approach, the ISDS can determine two or more cells each of which indicates a corresponding system cache having a copy of a memory line without the need of bit-vector information.

In addition, Applicant further claims in claim 1, using an Ingrained Sharing Directory Cache (ISDC) pending request queue. The ISDC pending request queue is separate from either

the ISDC or the ISDS. Specifically, Applicant claims "**storing an incoming operation request into the ISDC pending request queue**" when a "miss" occurs. This enables the ISDC to handle incoming ISDC operation requests concurrently without having to suspend operation while the ISDC is waiting for an ISDS data reply for a required status information for a memory line cached in two or more of the system caches.

Michael describes a system and method of maintaining consistent cached copies of memory in a multiprocessing system. Specifically, Michael describes a node comprising a memory directory having entries mapping a local main memory and a directory cache having entries corresponding to a subset of the cache directory entries.

Joseph describes a cache coherence controller in a distributed shared memory multiprocessing system. Specifically, Joseph describes using a pending buffers to maintain the status of memory transactions in progress.

Carpenter describes a method and system for evicting a cache line from a sparse directory within a non-uniform memory access computer system. Specifically, Carpenter describes using eviction buffers that hold an address of memory lines that are being evicted.

Applicant respectfully submits that none of the cited references, alone or in combination, teach or suggest using an ISDS that has a plurality of cells and "**each of the cells maintains a dynamic full map of shared lines cached in a given set of one of the plurality of system caches**" as taught by Applicant and claimed in claims 1, 10, 18, 32 and 35. Applicant also respectfully submits that none of the cited references, alone or in combination, teach or suggest "**storing an incoming operation request into the ISDC pending request queue**" when a 'miss' occurs as taught by Applicant and claimed in claim 1. Claims 1, 10, 18 and 35 have been amended to more clearly define Applicant's claimed invention.

First of all, regarding claims 1, 10, 18 and 35, Applicant's claimed invention enables determining two or more cells each of which indicates a corresponding system cache having a copy of a memory line without the need of bit-vector information as discussed above. Although Michael describes a cache directory (i.e., memory directory) of which entry is mapped into a corresponding entry for an associated system cache in the same node, Michael does not teach or suggest how each entry of the cache directory keeps track of a copy of a given local memory line

cached in a plurality of system caches throughout multiple nodes (*see* e.g., Fig. 8). Applicant is unable to find such a teaching in any of the cited references.

In addition, regarding claim 1, the Office Action states that although Michael fails to teach a pending buffer, combination of Joseph and Carpenter teaches or suggests use of the pending buffer as taught by Applicant and claimed in claim 1 (Office Action, p. 5, line 7 through p. 6, line 8). As support of this, the Office Action points to col. 1, lines 14-67 of Joseph, parts of which state:

> (col. 1, lines 15-17) The coherence controllers of cache coherent distributed shared memory multiprocessor systems use **pending buffers** to maintain the **status** of memory transactions in progress.
>
> (col. 1, lines 39-44) Each **pending buffer** entry 310 includes a valid bit 320, that indicates whether the contents of the entry are in use or not, an address 330 that indicates the memory lines to which the pending buffer entry corresponds if the valid bit is set to 'TRUE', and other **status** fields 340 that indicate the status of the addressed memory line.

The Examiner also points to col. 8, lines 28-55 of Carpenter, parts of which state:

> (col. 8, lines 31-33) ... As shown, eviction logic 60 includes three components, namely, eviction select logic 61, evict generate logic 62, and **eviction buffers** 63.
>
> (col. 8, lines 37-38) ... If all the entries within the coherency directory are in a **pending state**, an eviction-busy flag will be set...
>
> (col. 8, lines 45-48) ... In addition to holding the information about what response are required for the eviction to be completed, **eviction buffers** 63 **hold the address of the memory lines that are being evicted**...

Specifically, the Office Action states that "Joseph teaches putting a memory request in [a] pending buffer during memory transaction in progress i.e. in case of directory cache miss in the system of Michael, the request is stored in the pending buffer while awaits the required information being acquired from the memory directory" (p. 5, lines 18-21). The Office Action also argues that "it would have been obvious to one having ordinary skill in the art at the time of the invention to put in an eviction buffer (pending buffer) a memory transaction in progress such as replacing a cache line from memory directory as taught by Carpenter to maintain the coherency" (*Id.* p. 6, lines 2-8). For this, the Office Action assumes that the pending buffer in Joseph and the eviction buffer in Carpenter are equal to Applicant's ISDC pending request queue (Fig. 2, 208).

Applicant respectfully disagrees with the Examiner's interpretation of Joseph and Carpenter. First of all, as quoted above, the cited portion of Joseph simply shows that Joseph's pending buffer is a storage (e.g., cache) holding information for memory lines to be used by memory transactions in progress (i.e., pending transactions). For that purpose, Joseph's pending buffer maintains, for example, the **status** information for the memory transactions in progress. It is not clear from a reading of Joseph, however, whether Joseph's pending buffer stores a directory cache operation request itself into the pending buffer. Secondly, as quoted above, the cited portion of Carpenter simply shows that Carpenter's eviction buffer **holds the address of the memory lines that are being evicted**. The cited portion does not show that Carpenter's eviction buffer holds an incoming ISDC request itself.

In contrast, Applicant explicitly teaches at Fig. 8, block 822 and p. 19, lines 9-10, and claims in amended claim 1, **storing an incoming ISDC operation request into the ISDC pending request queue**. As discussed above, the use of the ISDC pending request queue enables concurrent handling of multiple incoming operation requests even while the ISDC is waiting for a data reply from the ISDS for a missed ISDC entry. Applicant is unable to find such a teaching in any of the cited references.

For the reasons discussed above, none of the references cited by the Examiner, alone or in combination, teach or suggest a method of maintaining cache coherency using an Ingrained Sharing Directory Cache (ISDC) as taught by Applicant and claimed in amended claims 1, 10, 18, 32 and 35. Reconsideration is respectfully requested.

Claims 3-5, 7, 9, 13-17, 22-24, 28-34 and 39-41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Michael et al. (U.S. Publication No. 2002/0002659A1), Joseph et al. (U.S. Patent No. 6,405,292) and Carpenter et al. (U.S. Patent No. 6,266,743) and further in view of Joseph et al. (U.S. Patent No. 6,338,123: hereinafter "Joseph 2").

Applicant invention claimed in amended claims 3, 7, 13, 22 and 39 pertains to using an Ingrained Sharing Directory Storage (ISDS) having a plurality of coherence buffers. Each of the coherence buffers maintains a dynamic full map of memory lines cached in a given set in system caches and evicted from an Ingrained Sharing Directory Cache (ISDC). Each of the coherence buffers maintains a plurality of cells. Each of the cells maintains a dynamic full map of shared

lines cached in a given set of a given system cache and evicted from the ISDC. Also, each of the cells maintains a plurality of entries and each of the entries comprises a memory address of an associated memory line.

Michael is discussed above.

Joseph is discussed above.

Carpenter is discussed above.

Joseph 2 describes using a Complete and Concise Remote (CCR) directory which employs a plurality of shadow directories. Each of the shadow directories includes only state information of the local main memory cached in the external shared caches (Abstract).

The Office Action states that although Michael, Joseph and Carpenter fail to teach, dynamic full map of memory lines as required by claim 3, Joseph 2 teaches dynamic full map directory keeping track of local memory lines in remote system caches (pp. 7-8, #8). As support of this, the Office Action points to col. 2, lines 17-49 of Joseph 2.

Applicant respectfully disagrees. Although Joseph 2's CCR directory provides a dynamic full map directory of presently shared lined in a plurality of external system caches, the CCR has different solution to do that. Under Joseph 2's approach, the CCR employs a plurality of separate shadow directories. Each of the shadow directories is associated with one external system cache. It is not clear, however, from a reading of Joseph 2 how the CCR directory determines a shadow directory and its entries to be used because the shadow directory includes only state information of a corresponding local main memory cached in the sharing external system caches and there.

In contrast, Applicant further teaches and claims in amended claims 3, 7, 13, 22 and 39, "selecting one of the coherence buffers based on a SELECT_CB field of an incoming address of an ISDS request; selecting one of the cells in the selected coherence buffer based on a SELECT_CELL field of the incoming address of the ISDS request, wherein a value of the SELECT_CELL field is associated with one of plurality system caches; and selecting an ISDS entry using a MEMORY_TAG field of the incoming address of the ISDS request."

For example, if two or more system caches have a copy of a given memory line, the ISDS has the same number of entries. Each of the entries has status information for the copied memory line in a corresponding system cache throughout multiple nodes. Under Applicant's claimed invention, as noted in the discussion of claims 1, 10, 18 and 35, the ISDS does not have to keep

bit-vector information for each entry to indicate the two or more system caches sharing the memory line since the ISDS entries are determined as a function of the indicator for the coherence buffers and the indicator for the cells. Applicant is unable to find such a teaching in any of the cited references.

For the reason discussed above, none of the references cited by the Examiner, alone or in combination, teach or suggest a method of maintaining cache coherency using an Ingrained Sharing Directory Cache (ISDC) as taught by Applicant and claimed in claims 3, 7, 13, 22 and 39. Claims 3, 7, 13, 22 and 39 have been amended to emphasize this difference. Reconsideration is respectfully requested.

Claims 6, 8, 25-27 and 42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Michael et al. (U.S. Publication No. 2002/0002659A1), Joseph et al. (U.S. Patent No. 6,405,292), Carpenter et al. (U.S. Patent No. 6,266,743) and Joseph et al. (U.S. Patent No. 6,338,123) as applied to claims 3, 7, 22 and 39 above and further in view of Lai (U.S. Patent No. 5,564,035). Claims 6, 8, 25 and 42 are patentable as being dependent on a patentable base claim.

Claims 2, 5, 9, 11, 12, 14-17, 19-21, 24, 36-38 and 41 are patentable as being dependent on a patentable base claim.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with

this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record is relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 21 day of May 2007.

KATE GAWRON

Name

Signature